**REMARKS**

A telephone discussion between the Examiner and Dennis Smid (one of the applicant's undersigned attorneys) was held on February 24, 2009. The applicant and Mr. Smid wish to thank the Examiner for his time and consideration for such discussion.

Claims 8 and 9 have been canceled. Claims 2-4, 6, 7, 12, and 14, amended claims 1, 5, 10, 11, and 13, and new claim 15 are in this application.

Claims 1-7 were rejected under 35 U.S.C. 112, second paragraph.

In explaining the above 112 rejection, the Examiner stated that in claims 1 and 5 the phrase "for outputting the same" is unclear. Claims 1 and 5 have been amended herein so as to delete such phrase. Accordingly, it is respectfully requested that the above 112 rejection of claims 1-7 be withdrawn.

Claims 1-7 were rejected under 35 U.S.C. 103(a) as being unpatentable over JP 02249333 (Hirade, Junji et al.) in view of U.S. Patent No. 3,784,743 A (Schroeder).

Each of independent claims 1 and 5 has been amended herein in the manner discussed during the February 24 discussion. As a result, and as an example, amended independent claim 1 now recites in part the following:

> "**data generating means** for generating bit data of a predetermined pattern and for supplying the generated bit data of the predetermined pattern to one or more of the shift registers and for outputting the generated bit data of the predetermined pattern; and

> **switching means** supplied with the scramble-processed data and the bit data of the predetermined pattern generated by the data generating means to select the bit data of the predetermined pattern at the time of synchronization processing of transmit data, and to select the scramble-processed data when synchronization processing of transmit data is not performed to output the data thus selected as scrambler output data,
>
> **the generated bit data of the predetermined pattern supplied to the one or more of the shift registers is the same as the generated bit data of the predetermined pattern supplied to the switching means**." (Emphasis added.)

It is believed that the present application provides support for the above-identified feature added to claim 1. With regard thereto, and as an example, reference is made to lines 3-10 of page 14 of the present application.

During the February 24 discussion, the Examiner indicated that the applied combination of Hirade and Schroeder does not appear to disclose the above-identified feature of claim 1.

Also, and as discussed during the February 24 discussion, in explaining the 103 rejection with regard to claim 1, the Examiner appears to assert that the first pseudo random signal generator of Hirade (which includes shift registers SR1-6 and switching circuit 2) is the same as the data generating means of claim 1, and that the switching circuit 2 of Hirade is the same as the switching means of claim 1.

As discussed during the February 24 discussion, it is respectfully submitted that switching circuit 2 of Hirade is not the same as the switching means of claim 1. As an example, the switching means of claim 1 may be supplied with (i) scramble-processed data and (ii) the bit data of the predetermined

pattern generated by the data generating means; and the switching means of claim 1 may select the bit data of the predetermined pattern at the time of synchronization processing of transmit data and the scramble-processed data when synchronization processing of transmit data is not performed. On the other hand, the switching circuit 2 of Hirade does not appear to be supplied with scramble-processed data and, as such, is believed to be substantially different from the switching means of claim 1.

Accordingly, it is respectfully requested that the above 103 rejection of claim 1 be withdrawn.

For reasons similar to or somewhat similar to those previously described with regard to claim 1, it is also respectfully requested that the above 103 rejection of amended independent claim 5 be withdrawn.

Claims 2-4, 6, and 7 are dependent from one of independent claims 1 and 5. Accordingly, it is also respectfully requested that the above 103 rejection of claims 2-4, 6, and 7 be withdrawn for at least the reasons previously described.

Claims 10-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,535,239 A (Padovani et al.) in view of Schroeder.

Amended independent claim 10 now recites in part the following:

> "a random number generating circuit to generate a random bit data train, said random number generating circuit having a first shift register, a second shift register, and a first adder . . .;
>
> a data generator to generate bit data of a predetermined pattern and to supply the generated bit data of the predetermined pattern therefrom, **said data generator being**

> **separate from the random number generating circuit**;
>
> a second adder arranged to receive an output of the first adder and the transmit data and being operable to generate scramble-processed data therefrom;
>
> **a first switch arranged to receive the scramble-processed data from the second adder and the bit data of the predetermined pattern from the data generator**, said first switch being operable to select the bit data of the predetermined pattern at the time of synchronization processing of the transmit data and to select the scramble-processed data when synchronization processing of the transmit data is not performed and to output the data selected." (Emphasis added.)

It is respectfully submitted that the applied combination of Padovani and Schroeder does not appear to disclose all of the above-identified features now recited in claim 10. As an example, such applied combination of Padovani and Schroeder does not appear to disclose "a random number generating circuit" and "a data generator . . . [which is] separate from the random number generating circuit" along with "a first switch arranged to receive the scramble-processed data from the second adder and the bit data of the predetermined pattern from the data generator" as in claim 10. As best understood, in explaining the above 103 rejection with regard to claim 10, the Examiner appears to assert that Padovani (and in particular, elements 62, 64, and 66 of Fig. 3 thereof) are the same as the random number generating circuit of claim 10, that Padovani discloses the data generator of claim 10, and that Schroeder (and in particular Fig. 1 thereof) discloses the first switch of claim 10. In response, and as an example, it is respectfully submitted that such portion of Schroeder does not appear to disclose the first switch as specifically recited in

claim 10.

Accordingly, it is respectfully requested that the above 103 rejection of claim 10 be withdrawn.

Claims 11-14 are dependent from independent claim 10. Accordingly, it is also respectfully requested that the above 103 rejection of claims 11-14 be withdrawn for at least the reasons previously described.

Further, and as discussed during the February 24 discussion, new independent claim 15 has been added herein.

Furthermore, and as discussed during the February 24 discussion, a Request for Continued Examination accompanies this Amendment.

As it is believed that all of the rejections set forth in the Official Action have been overcome, favorable reconsideration and allowance are earnestly solicited. If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that the Examiner telephone applicant's attorney at (908) 654-5000 in order to overcome any additional rejections and/or objections which the Examiner might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

By _____

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